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The main focus of the program is the development of ultrafast superconductor devices and circuits based on the storage, transfer and processing of digital bits encoded by single quanta of magnetic flux. This approach offers several key advantages ovser other possible digital superconductor technologies, most importantly an extremely high operation speed. During the first period of the program, substantial progress in the development of these Rapid Single-Flux-Quantum (RSFQ) devices and circuits was achieved. In particular: ballistic transfer of SFQ signals over distances of up to 1 cm, and logic operation with very low error probability (below 10^{-15} bit^{-1}) were demonstrated experimentally; a comprehensive library of RSFQ logic gates and auxiliary components were designed, optimized, and tested experimentally; several RSFQ circuits of modest integration scale (a few hundres Josephson junctions) were designed and successfully tested; a new fabrication technology featuring 1.5 um high-j_c Josephson junctions was developed and used to implement an RSFQ circuit operating at record speed (up to 370 GHz). Simultaneously, important improvements were made in design, fabrication, and testing capabilities. Also a group of some 12 undergraduate and graduate students have received substantial training in various aspects of superconductor electronics.

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Multidisciplinary Block Program

ADVANCED SUPERCONDUCTOR DIGITAL ELECTRONICS

DoD's University Research Initiative
Multi-Agency Topic
"Low-Temperature Superconductor Digital Electronics"

(AFOSR Grant # F49620-92-J-0508)

Final Report

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Contents

Executive Summary

The 5-year multidisciplinary program *Advanced Superconductor Digital Electronics* within the framework of DoD's University Research Initiative was started at Stony Brook in September 1992. During the first 3-year stage (later extended for one more year without additional funds) it was supported via the AFOSR Grant #F49620-92-J-0508.

The main focus of the program is the development of ultrafast superconductor devices and circuits based on the storage, transfer, and processing of digital bits encoded by single quanta of magnetic flux. This approach offers several key advantages over other possible digital superconductor technologies, most importantly an extremely high operation speed. During the first period of the program, substantial progress in the development of these Rapid Single-Flux-Quantum (RSFQ) devices and circuits was achieved. In particular:

- ballistic transfer of SFQ signals over distances of up to 1 cm, and logic operation with very low error probability (below 10^{-15} bit^{-1}) were demonstrated experimentally;
- a comprehensive library of RSFQ logic gates and auxiliary components was designed, optimized, and tested experimentally;
- several RSFQ circuits of modest integration scale (a few hundred Josephson junctions) were designed and successfully tested;
- a new fabrication technology featuring 1.5-μm high-j_c Josephson junctions was developed and used to implement an RSFQ circuit operating at record speed (up to 370 GHz).

Simultaneously, important improvements were made in design, fabrication, and testing capabilities. Also, a group of some 12 undergraduate and graduate students have received substantial training in various aspects of superconductor electronics. We believe that the original goals of this period have generally been met, and in some areas, surpassed.

This background should allow us to achieve important goals during the current, second stage of the program. Most importantly, we are going to demonstrate laboratory prototypes of at least three integrated circuits (A/D converter, digital SQUID, and digital autocorrelator) with performance much higher than those of their commercially available counterparts. We also plan to demonstrate several new ultrafast subsystems using the RSFQ technology, including a digital signal processor unit, a general circuit microprocessor with on-chip cache memory, and a digital switch. We are also going to develop a new fabrication technology featuring non-hysteretic submicron Josephson junctions which will enable us not only to approach 1 THz operation speed in simple RSFQ circuits, but also to increase the density of the circuits at least tenfold.

1. Introduction: RSFQ Technology and Stony Brook Program

The main focus of our program is the development of ultrafast superconductor digital devices and circuits of the Rapid Single-Flux-Quantum family (for reviews, see Refs. 1, 2). In this family of devices, the binary information is stored in superconducting loops in the form of the number N of trapped quanta of magnetic flux:

$$\Phi = N\Phi_0, \qquad N = \text{either 0 or 1}, \qquad \Phi_0 = h/2e \approx 2\text{x}10^{-15}\ \text{Wb}. \quad (1)$$

The loops include one or several overdamped Josephson junctions which allow the state N of the loop to be changed (i.e. a single flux quantum injected or extracted) during a very short time interval τ. This interval is limited by the ratio of capacitance C of the Josephson junction to its critical current I_c and ultimately by the superconductor energy gap $\Delta(T)$:

$$\tau \approx \max[(\pi\Phi_0 C/2I_c)^{1/2};\ \pi\hbar/4\Delta(0)], \quad (2)$$

For present-day low-T_c Josephson junction technologies, τ is of the order of a few picoseconds (see Table 1 below).

A change in flux Φ in the loop by Φ_0 results in the formation of a picosecond "Single-Flux-Quantum" (SFQ) pulse of voltage V(t) with the quantized area

$$\int V(t)\, dt = \Phi_0 \approx 2\ \text{mV-ps}. \quad (3)$$

In circuits of the RSFQ family, these picosecond pulses are used for the transfer and processing of the binary information. The logic gates ("elementary cells") of this family have natural intrinsic memory and may be clocked by SFQ pulses [1, 2]. The advantages of this approach include:

- a natural reset of logic gates on the picosecond time scale;
- possibility of data transfer at a speed approaching that of light;
- flexible combination of synchronous and asynchronous timing;
- dc power supply.

Theoretical analysis shows [1, 2] that these features allow the implementation of complex RSFQ circuits with extremely high clock frequencies, potentially in excess of 300 GHz, i.e. some three orders of magnitude higher than that of the fastest semiconductor VLSI circuits. Other advantages of the RSFQ approach include very small power consumption (fundamentally limited only by thermal fluctuations, at helium temperatures to ~10^{-19} J/bit) and relatively simple fabrication technology.

The main problem with low-T_c RSFQ technology is the necessity of helium cooling which is very inconvenient for many potential users. Possible solutions to this problem include:

- reaching a decisive leading edge in performance (first of all, in speed) which would outweigh the burdens of refrigeration;
- targeting niche applications where liquid helium is used anyway (e.g., magnetic resonance imaging, SQUID magnetometry, etc.);
- development of more efficient and simple helium range refrigerators;
- gradual transfer of the technology to higher temperatures, as soon as the technology of high-T_c Josephson junctions matures.

It is possible that the eventual introduction of the RSFQ technology to practice would require a combination of these approaches.

In the initial proposal of our multidisciplinary program, the basic goal was formulated as follows: "*to pave the way to practical superconductor circuits and systems based on* [RSFQ] *devices*". Initially the first stage of the program included 36 interrelated research projects leading to this final goal; of those, work on 26 projects was eventually funded. During the 4 years of the program, some 300 RSFQ circuits were analyzed, designed, fabricated, and tested. What follows is a list of the main results in the major directions of our work.

2. Main Scientific Results

A. Fundamentals and Logistics

A.1. Experiments with SFQ pulses

Since the inception of the RSFQ approach in 1985, its basic concepts have been repeatedly questioned. The most frequently used argument was that the millivolt, picosecond SFQ pulses were so "weak" that switching using them might not be reliable. Though these doubts had not been confirmed by any theoretical analysis, we found it necessary to carry out several special experiments to refute them.

In the first experiment [3], we demonstrated the ballistic transfer of SFQ pulses over 1-cm long passive superconductor microstrip lines, without noticeable attenuation. The experimental circuit consisted of a DC/SFQ converter, a special driver, a 20-μm-wide microstrip line, a special receiver, and two SFQ monitors (SFQ/DC converters nesting on T flip-flops). An additional monitor was used to control input SFQ pulses. Within our experimental accuracy (~30%) we could not detect any decrease of the pulse amplitude after its transfer

through 1-cm lines with as many as 18 turns. This implies that SFQ pulses can be ballistically transferred between any points of complex integrated circuits.

In another series of experiments [19] we demonstrated that RSFQ devices can have a very low rate of digital errors. In these experiments, an SFQ pulse might travel around a loop formed by an RSFQ Inverter (with the SFQ pulse fed into the clock input), Josephson transmission line, and a confluence buffer, at frequency f~10-20 GHz. We were able to measure the error rate within the range 10^{-4}-10^{+4} s^{-1} by monitoring the voltage across any junction of the transmission line. The errors were clearly observed at the margins of the parameter window. However, in the middle of the window we did not register any error during a 6-hour continuous run, which leads to the upper bound of $3x10^{-15}$ 1/bit for the error rate. Later, we repeated the same experiment at a higher frequency, and reduced the upper bound even further (down to 10^{-15} 1/bit).

Estimates based on the assumption of thermal activation dominance yield an extremely low error rate (between 10^{-50} and 10^{-100} bit^{-1}) for our circuit parameters. In order to check the validity of this assumption, in a separate experiment [4] we measured fluctuation-induced width ΔI_X of the switching threshold of a key component of the RSFQ circuits, the balanced comparator. The measured width values (close to 10 μA at 4.2K) were found to be in excellent agreement with the results of theory based on purely thermal activation. This result implies that the error rate in RSFQ circuits may be low enough for all planned applications. Recently, we extended these theoretical and experimental studies to the case of finite time interval between the input pulses [32]. The results indicate that "smoothing" of the shape of the input pulses may decrease ΔI_X substantially (typically, by a factor of ~3) and as a result increase the effective parameter margins of RSFQ devices and circuits.

One more confirmation of the fact that the effects of technical fluctuations in circuits may be negligibly small, has come from an experiment with the RSFQ clock circuit [5]. This circuit included an RSFQ ring oscillator with frequency f_0 in the range 30-100 GHz and a frequency divider by $N=2^{24}\approx1.5x10^7$. The stability of the frequency $f=f_0/N\approx$2-6 kHz of the resulting signal was studied using both time-domain and frequency-domain techniques. The relative jitter of the low frequency oscillation period was found to be smaller than 10^{-4}. This result implies that the effective amplitude of low-frequency technical fluctuations of currents flowing through the junctions is below ~ 0.01 μA, i.e. much lower than the r.m.s. thermal fluctuation current (~0.18 μA at 4.2 K), and hence their effect is negligible.

To summarize, we believe that our experiments with SFQ pulses (as well as successful implementation of relatively complex RSFQ circuits, see Sec. C below) have convincingly confirmed the basic concepts of the RSFQ approach.

A2. Interfacing Superconductor and Semiconductor Electronics

We have developed and tested simple and reliable electronics for interfacing RSFQ circuits to room-temperature semiconductor digital electronics [6]. The interface is based on the conversion of picosecond SFQ pulses into ~150-μV voltage levels by special non-latching Josephson junction circuits ("SFQ-DC converters"), optional amplification of the levels to ~1.5 mV by a HUFFLE-type dc-biased latching circuit, transfer of the resulting signals to room-temperature in the return-to-zero format via commercially available coplanar waveguides, amplification of the signals by simple room-temperature semiconductor amplifiers to the standard bipolar level, and finally using silicon bipolar flip-flops for conversion of the signals to the standard non-return-to-zero (voltage-level) format. In particular, we have developed a single-bit interface (with the HUFFLE amplifier) which allows reliable operation at data rates up to ~1 Gbps, and a 20-channel interface (without HUFFLE amplifiers) operating at a data rate above 30 Mbps per channel. Due to the absence of expensive low-temperature semiconductor amplifiers, the cost of parts for the interface as a whole is below $20 per channel.

A3. Experimental Capability Development

We have developed and introduced several experimental setups for testing RSFQ devices and circuits at low and high (up to 1 GHz) frequencies. The highlight of this development is an advanced 64-channel system (presently called OCTOPUX) for automated testing of complex superconductor circuits at relatively low frequencies (up to ~300 kHz) [37]. The system features ~100-fold advantage in speed over our previous system OCTOPUS [7]. Besides the regular measurement procedures using 16-bit D/A and 12-bit A/D converters, the system allows the high-power supply (up to 1A at 10 V) of up to 6 channels, and high-precision measurement of signals from selected channels using the incorporated Keithley 2001 multimeter.

A4. Design Capability Development

We have developed [33] several important additions to our original PSCAN circuit simulator, and improved the software package (called L-METER) for automated calculation of mutual and self-inductance matrices for arbitrary fragments of multi-layered superconductor circuits and structures [8, 9]. Presently, all these tools are available in both MS-DOS and UNIX versions, and are run at various platforms. Nevertheless we have found these tools to be insufficient for the development of complex RSFQ systems. This is why we leased the industrial-grade CAD system CADENCE, and developed adequate interfaces and technology files which allow us to use PSCAN and L-METER as additional CADENCE tools. These developments have improved our design productivity dramatically.

B. Fabrication Technology and Josephson Junction Physics

B1. 1.5-μm Nb-Trilayer Technology

During the first two years of our program, we mostly used the fabrication technology of HYPRES, Inc. for experimental implementation of our devices and circuits. This niobium foundry service is probably the best available in the United States, and features fast turnaround, well formulated design rules, relatively low cost, and helpful and knowledgeable staff. Nevertheless, the basic fabrication technology of HYPRES is rather conservative, with Josephson junction size no smaller than 3.5-μm. Capacitance C of these junctions is relatively high, resulting, according to Eq. (2), in relatively long SFQ pulses - see Table 1 [2, 39].

Table 1. Basic parameters of some Nb-trilayer fabrication technologies

Parameters	HYPRES, Inc.	SUNY Present	Prospective
Josephson Junction Size (μm)	3.5	1.5	0.3
Critical Current Density (kA/cm^2)	1	6	100
SFQ Pulse Duration (ps)	4	2	0.6
Clock Frequency of Complex RSFQ Circuits (GHz)	20-40	40-80	100-200

Hence an important direction of our program is the development of an advanced Nb-trilayer fabrication technology at Stony Brook. The first generation of this technology features 1.5-μm Josephson junctions with critical current density close to 6 kA/cm^2 (Table 1). The main new feature of this technology is planarisation, based on chemical-mechanical polishing, for the fabrication of Josephson junction circuits with small junction area and high critical current density [10, 11, 35].

For the first test of the technology we used [12] a simple RSFQ circuit consisting of a generator of a continuous train of SFQ pulses, Josephson

transmission line, and T flip-flop (i.e., a single-stage asynchronous binary counter). The correct operation of the flip-flop (i.e. division of frequency of the incident pulse train by 2), could be confirmed by comparison of dc voltages across the SFQ pulse generator, and one of the junctions of the T flip-flop. The measurements showed that circuits from various wafers operated correctly at input frequencies up to 370 GHz, in fair agreement with the results of numerical simulation of the circuit using the microscopic "Werthamer" model of the Josephson junctions. The achieved division frequency is a factor of 2.5 larger than that reported previously (using HYPRES technology), and is much higher than the speed of any digital device based on an alternative digital technology. These experiments have confirmed the expected scaling of the RSFQ circuits and imply that using the full scale of our technology (with 3 superconducting layers) we shall be able to fabricate much more complex RSFQ circuits with maximum clock frequencies above 100 GHz.

Using the full scale process, we have fabricated and successfully tested several RSFQ circuits with up to 60 Josephson junctions, though we are still problems with microshorts between the upper superconducting layers of the circuits. In order to solve the problem, we are replacing SiO insulation between these layers with SiO_2, which should provide better step coverage [35].

B2. Submicron Nb-Trilayer Technology

We have also started to work on a deep-submicron version of the planarized technology, using electron beam lithography for Josephson junction definition. We have been able to demonstrate single Josephson junctions with effective area down to 0.006 μm^2 and critical current density beyond 300 kA/cm^2 [13]. These junctions exhibit non-hysteretic I-V curves with very respectable $I_C R_N$ product of the order of 1 mV (corresponding to an expected 500-GHz speed of simple RSFQ circuits). Their I-V curves, however, differ substantially from those predicted by existing theories of the Josephson effect in tunnel junctions (such deviations were reported earlier by other authors for lower values of j_C).

B3. Josephson Effect in Mesoscopic Channels

In order to understand the origin of these differences we have developed a microscopic theory of ac Josephson effect in a single quantum channel of arbitrary transparency D [14, 15, 34]. The theory, valid for arbitrary temperatures, gives all components of the current through the channel as functions of dc voltage between the superconductor electrodes. For small transparency ($D<<1$) the results coincide with the well-known Werthamer-Larkin-Ovchinnikov theory for tunnel junctions. For $D\sim1$ the new theory shows, however, considerable deviations from the tunnel behavior; these deviations are qualitatively similar to those observed experimentally in our high-j_C junctions. We

hope that further development of the theory, in particular its generalization to mesoscopic contacts with several quantum channels, will allow us to reach a good understanding of such junctions.

On the experimental side, we began a project directed toward the experimental observation of the mesoscopic contacts in niobium trilayers using scanning tunnel microscopy (STM). The idea is to perform STM imaging of the Nb/Al bilayer *in situ* immediately before and right after oxidation of the aluminum layer, and then to subtract the images electronically to map the AlO_x transparency with atomic-scale resolution. We have already achieved reliable operation of an STM in one of our thin film deposition chambers, and are close to the first run of the experiment as a whole.

B4. S-N Junction Cryocooling

As an unexpected by-product of our work on the theory of Josephson junctions we ran into an opportunity for very efficient thermoelectric cooling based on quasiparticle transfer through SIN junctions [16]. In collaboration with a Finnish group we have demonstrated cooling from 300 to 100 mK, using a pair of small-size junctions $Cu/CuO_x/Al$ [17]. Preliminary estimates show that using a superconductor with wider energy gap (e.g. niobium), a refrigeration power of ~100 mW may be reached at 4 K using a 1-mm^2 junction. We plan to complete a feasibility study of this opportunity in the near future.

B5. All-High-T_c RSFQ Circuit

We have used design and testing capabilities developed during this program to collaborate with Prof. Gurvitch's group in the development and testing of the first all-high-T_c RSFQ circuit. The circuit, comprising 14 Josephson junctions formed by direct e-beam writing, included 2 DC/SFQ converters, 2 Josephson transmission lines, SFQ RS flip-flop, and an SFQ/DC converter. Reliable operation of the circuit at temperatures close to 30 K has been demonstrated [18]. According to our estimates, similar circuits should operate with a relatively low error rate at liquid nitrogen temperatures. In order to implement more complex digital circuits, however, the high-T_c Josephson junction technology has to be substantially improved.

C. Development of RSFQ Devices, Circuits, and Systems

C1. RSFQ Library

An important direction of our work during the first two years was the development of the basic library of RSFQ components, logic gates, and auxiliary circuits. Though some experiments with RSFQ devices had been carried out

before the beginning of our program [1], the list was rather short, and performance far from ultimate. That is why we have found it necessary to re-design, re-optimize, and re-test experimentally all the previously suggested devices and components, and to add many new devices to the library [19-31].

A highlight of this development was the introduction [20] of a new family of RSFQ circuits based on a single template called B Flip-Flop. The template is a bistable SFQ circuit with up to 4 inputs and 6 outputs. An SFQ pulse arriving at a particular input results in the generation of two SFQ pulses at a particular pair of its outputs. Minor modifications of the template circuit give a broad variety of single-bit RSFQ circuits performing various 2-operand logic functions. An important advantage of these circuits is their high parameter tolerance, with the critical margin typically close to 30%. Their disadvantage is lower speed: the maximum clock frequency of the B Flip-Flop is of the order of 30 GHz for 3.5-μm Josephson junction technology, i.e. about twice as low as that for the fastest RSFQ circuits implemented using the same technology. We use devices of the B-Flip-Flop family in the bulk of RSFQ integrated circuits, while faster (though less convenient) custom-designed devices are used in bottlenecks limiting the overall speed.

Another important achievement was the development of internally-tristable logic elements which look from the outside like normal bistable logic gates. This method allows considerable hardware savings at implementation of several logic functions [21].

C2. A/D Converters

Our first system goal is an SFQ-counting 16-bit A/D converter, with sampling rate ~20 GHz and a signal bandwidth much wider than in its semiconductor counterparts [22-25]. Its basic blocks including decimation ("comb") filter [23], input circuit with an original quantizer of the analog signal [24], and clock controller [5] have already been developed, fabricated and tested [25]. Experimental assembly and testing of the full A/D is the goal of the second (2-year) stage of our project.

C3. Digital SQUIDs

Most blocks of the A/D converter, notably the digital decimation filter, may be used to design a digital SQUID with a very high slew rate (~10^{10} Φ_0/s), which could be used in unshielded environments (e.g. for biomagnetic measurements and non-destructive evaluation). Presently, all the basic blocks of the first prototype of the SQUID (including its interface with room-temperature electronics) have been designed. We expect to assemble and test the whole system during the second stage of our program.

C4. D/A Converters

We have designed and successfully tested a simple (3-bit) prototype of an RSFQ D/A converter [26]. Such converters may combine an unprecedented accuracy of each voltage level (unlimited fundamentally at least up to ~10^{-15}) with a reasonable bit number n and broad band (e.g., n=18 bits at 1 MHz). In order to implement such a high resolution, the Josephson number count has to be quite large ($N \sim 2^{n+2} \sim 10^6$), necessarily involving multi-chip systems. During the second stage of our program we plan to demonstrate a full laboratory prototype of a 20-bit D/A system.

C5. Digital Autocorrelators

We have begun the development of digital autocorrelators with extremely wide signal band (8 GHz in the first version), and have already designed and tested the basic cells of the system, including a 3-stage delay line and 4x4 array of accumulators [36]. A further increase in the number of channels will require a multi-chip system with 3-channel 48-Gbps communication line between the chips. We have already started to design a special cryogenic printed circuit board and interfaces for such a system, and hope to demonstrate the operation of the full autocorrelator at the second stage of our program.

C6. Digital Signal Processing

We are considering RSFQ implementation of several possible signal processing algorithms used in digital image processing, including digital cosine transform and motion estimation. The final choice has not yet been made, because we decided we needed to study the feasibility of RSFQ implementation of the basic building blocks of DSP systems. This is why we have designed an RSFQ bit-serial real-time multiplier. In contrast to earlier versions of RSFQ multipliers, this circuit has a simple modular structure with only 96 Josephson junctions per module, 28 μW power dissipation, and a calculated maximum clock frequency of 25 GHz (for 1-kA/cm^2 Josephson junctions). We have successfully tested (at low frequencies) all the RSFQ cells of the module and verified correct operation of its simplified version [27].

C7. Digital Packet Switching

The unique speed of RSFQ circuits may be used in packet switches for multiprocessor computers and communication systems. In preparation for this work, we (in collaboration with Tektronix and MSU groups) have designed and successfully tested an RSFQ version of a very common block of the switching systems, a decoder [28].

On the theoretical level, we have explored several opportunities to implement self-routing packet switching cores, with a simultaneous analysis of

the system, circuit, and device levels. The candidate structures included crossbar, Batcher-banyan, token ring, and shared bus. It has been found [38] that the Batcher-banyan architecture may require the lowest Josephson junction count at the fixed throughput. For example, with the 1.5-μm technology, the over throughput of 7.5 Tbps can be maintained with as few as ~170K junctions which may fit on a single 1x1-cm^2 chip. Laboratory prototypes of such switching core will be implemented during the second stage of our program.

C8. General-Purpose Computing

General-purpose computing requires a large memory, which typically cannot be placed on the processor chip. Time-of-flight provides a lower bound for the access time of such memories, of the order of 1 ns. For these reasons, the speed advantage of RSFQ circuits (in comparison with, say, GaAs or Josephson junction latching circuits) is less important in this area. However, another advantage of RSFQ circuits, their very low power consumption, becomes important, especially for very large computing systems. For example, a petaFLOPS-range RSFQ system would dissipate ~100 W at 4K (equivalent to ~30 kW at room temperature); the number to be compared with ~30 MW estimate for the best prospective CMOS systems of a similar performance [39].

Consequently we started a project directed toward the implementation of a prototype general-purpose computing system consisting of an RSFQ microprocessor chip and several (2 or more) Josephson junction memory chips. After thorough analysis, we have selected a particular architecture of a simple RISC microprocessor [29, 40] with 16-bit words, which would be able to implement 16 different instructions. According to our estimates, the microprocessor would operate at ~20 GHz internal clock frequency and have ~1-GHz frequency of exchange with external 8K memory.

We are considering several options for the memory chips. One option is to use two 4K chips from the NEC team, based on the latching logic; another is to find a combination of non-latching and latching circuits, which would exclude the necessity of gigahertz-frequency ac power supply (which gives a lot of trouble in practice). As a preliminary step, we have developed and tested all the basic components of a completely-RSFQ memory [30], with a very small (~80 λ^2) cell area.

We plan to design and test a full laboratory prototype of the microprocessor during the second stage of our project.

3. Educational Dimension

Besides purely scientific goals, our project proposal promised "to make strong emphasis on the educational side of the program", and in particular to improve [students'] education by stimulating the multi-disciplinary character of their projects".

We feel that we have been able to make good of this promise. During the first 4 years of the program, 12 talented students, both undergraduate and graduate, from several departments of SUNY Stony Brook:

Z. Bao (Physics)
A. Bardas (Physics)
P. Bunyk (Computer Science)
H. Imam (Physics)
A. Imitaz (Physics)
M. Kessler (Physics)
J.C. Lin (Electrical Engineering)
S. Polonsky (Physics)
A. Rylyakov (Physics)
V. Patel (Physics)
D. Schneider (Electrical Engineering)
D. Zinoviev (Computer Science)

received substantial training in various aspects of superconductor electronics. Despite the listed affiliation with a certain department, almost each student participated in really multi-disciplinary work. For example, the research work of Paul Bunyk (graduate student in Computer Science) included:

- design of the first RSFQ general purpose microprocessor [29],
- development of L-METER software package [8, 9], and
- design and experimental testing of first 1.5-μm RSFQ circuits [12].

We believe that such broad training will be extremely beneficial for the success of these young researchers in the diversified technological environment of the future.

4. Conclusion

To summarize, we believe that the basic goals of the first, 4-year stage our program have been successfully reached, and some of them have been surpassed. They have formed a reliable foundation for a successful conclusion of the 5-year program as a whole.

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